UNITED STATES PATENT APPLICATION

FOR

POWER MANAGED BUSSES AND ARBITRATION

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POWER MANAGED BUSSES AND ARBITRATION

Field Of The Invention

The present invention pertains to the field of computer systems. More particularly, this invention pertains to the field of power management of devices within computer systems.

Background of the Invention

In many semiconductor devices such as embedded processors, systems-on-a-chip (SOC), or other computer systems or consumer electronic devices, on-chip busses are becoming faster and wider with many associated register queues and related logic in attached unit interfaces. Split transaction capabilities on these busses have added significant depth to these queues. This is leading to a situation where on-chip busses and their associated interfaces will become a significant portion of overall system power, particularly in SOC designs.

In prior systems, power management may include simply reducing clock frequency for portions of the system (e.g., host processor), stopping clocks to unused logic units, or reducing clock frequency for the entire system, including busses. Another technique that is used is to throttle the clock off and on rather than slowing the clock down. These prior systems do not provide throttling of shared system resources such as backbone busses based on bandwidth demands and do not provide adjustments to arbitration configuration to provide sustained and stable bandwidth allocations despite aggregate bandwidth reductions.

Brief Description of the Drawings

The invention will be understood more fully from the detailed description given below and from the accompanying drawings of embodiments of the invention which, however, should not be taken to limit the invention to the specific embodiments described, but are for explanation and understanding only.

Figure 1 is a block diagram of one embodiment of a system including several functional units and an arbitration and bus clock control unit coupled to a variable speed bus.

Figure 2 is a flow diagram of one embodiment of a method for power managing a variable speed bus and adjusting arbitration configuration.

Detailed Description

In general, one embodiment of the invention involves throttling a bus frequency based upon bandwidth requirements of active units coupled to a variable speed bus. As units coupled to the bus are stopped, bandwidth requirements are lowered and the bus frequency is reduced in response to the lowered bandwidth requirements in order to reduce power consumption. Further, an arbiter selects an appropriate arbitration configuration based on which units are active and which are stopped. The arbitration configuration is adjusted to ensure that the bandwidth requirements of the active units are sustained despite reduced clock frequency.

The embodiments described herein discuss power management of shared resources such as busses by modulating bus frequency and adjusting arbiter configuration depending on current shared resource utilization. A wide range of techniques may be used to power manage the individual units or devices coupled to the bus.

Figure 1 is a block diagram of an example system 100 including a host processor unit 110, a graphics processor unit 120, a peripheral device controller 130, a video processor unit 140, an arbiter and bus clock controller 150, and a memory 160 coupled to a variable speed bus 155. The frequency of the variable speed bus 155 is controlled by the arbitration and bus clock controller 150. The system 100 is merely one of a large range of possible system configurations. The system 100 may be implemented on a single integrated circuit die, or may be implemented as discrete devices coupled to a bus.

For this example embodiment, the host processor 110 may require 700MB/s bandwidth when active. The graphics processor 120 may require 300MB/s of bandwidth when active. The peripheral device controller 130 may require 100MB/s of bandwidth

when active. The video processor may require 900MB/s of bandwidth when active. The variable speed bus 155 may be a 64bit wide bus having a top frequency of 250MHz, yielding a maximum of 2GB/s of available bandwidth. If all of the units 110, 120, 130, and 140 are active, the arbiter selects a configuration A which allocates 7 of 20 arbitration slots to the host processor 110, 3 of 20 arbitration slots to the graphics processor 120, 1 of 20 arbitration slots to the peripheral device controller 130, and 9 of 20 arbitration slots to the video processor 140.

For the current example, if the host processor 110 and graphics processor 120 are not used or are in a very low use state, such as when performing continuous video playback (watching a movie) using the peripheral controller 130 and the video processor 140, the variable speed bus may have as much as 1GB/s of unused bandwidth. In this scenario, the variable speed bus 155 can reduce its frequency by 50%. In order to ensure that the video processor continues to receive its required 900MB/s of bandwidth, the arbiter 150 selects a configuration B that provides 9 of 10 possible arbitration slots to the video processor 140. The peripheral controller 130 receives the remaining 1 of 10 arbitration slots to ensure that it receives its required 100MB/s bandwidth.

Continuing with the current example, it is possible that the video processor 140 may switch its bandwidth requirements from 900MB/s to 100MB/s. The variable speed bus 155 frequency can now be reduced to 200MB/s and the arbiter can change to a configuration where the video processor 140 is allocated 1 of 2 possible arbitration slots and the peripheral device controller 130 also receives 1 of 2 arbitration slots in order to ensure that each of the video processor 140 and the peripheral device controller 130 receive their required 100MB/s of bandwidth.

Another example of a situation that can benefit from being able to adjust both bus frequency and arbitration configuration is the situation where the host processor 110 is working mainly out of its cache. To load the cache, the variable speed bus 155 can increase its clock frequency in order to support the 700MB/s required by the host processor. Once the cache has been loaded and the processor is working mainly out of its cache, the bus frequency can be reduced and the arbiter can adjust its configuration to take into account the processor's lack of activity on the bus 155.

Figure 2 is a flow diagram of one embodiment of a method for power managing a variable speed bus and adjusting arbitration configuration. At block 210, a determination is made as to which of a plurality of units coupled to a variable speed bus are active. The clock frequency of the variable speed bus is adjusted according to the bandwidth requirements of the active units at block 220. At block 230, one of a plurality of arbiter configurations is selected depending on which of the plurality of units coupled to the variable speed bus are active.

In the foregoing specification the invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the appended claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than in a restrictive sense.

Reference in the specification to "an embodiment," "one embodiment," "some embodiments," or "other embodiments" means that a particular feature, structure, or characteristic described in connection with the embodiments is included in at least some

embodiments, but not necessarily all embodiments, of the invention. The various appearances of "an embodiment," "one embodiment," or "some embodiments" are not necessarily all referring to the same embodiments.